Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2698	central adj processing and (nonvolatile or non adj volatile) and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:37
L2	5042	cpu and (nonvolatile or non adj volatile) and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:37
L3	5459	1 or 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:37
L4	346	3 and program and fetch$3 with program	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:38
L5	122	4 and bit adj lines and word adj lines and memory adj cells	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:40
L6	21049	5 and potential during with predetermined adj period	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:41
L7	0	5 and potential with during with predetermined adj period	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:41
L8	0	5 and during with predetermined adj period	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:42

L9	1	5 and predetermined adj period	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:46
L10	100	5 and complementary	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:46
L11	92	10 and cell with gate with word adj line	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:47
L12	42	11 and predetermined adj voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:49
L13	0	12 and cell with pair with transistors	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:49
L14	8743	cell with pair with transistors	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:49
L15	8743	cell with pair with transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:50
L16	185	15 and 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:50

L17	102	16 and complementary	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 16:00
L18	163	17 @pd<"02202002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:52
L19	0	17 and @pd<"02202002"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:52
L20	1	17 and memory adj cell with pair adj transistor$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:56
L21	509	memory adj cell with pair adj transistor$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:56
L22	8	21 and 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 15:56
L23	0	3 and complementary adj bit adj line$1 near4 connected near5 differential adj amplifier$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 16:06
L24	19	3 and complementary adj bit adj line$1 near4 amplifier$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/14 16:06